a charge storage layer included in said first gate insulating film and absent from said second gate insulating film,

wherein said first and second transistors are isolated by a trench, said charge storage layer in said first transistor is restricted from an element isolation region and exists only below said first gate electrode in an element region, and a height of said charge storage layer above the semiconductor substrate is lower than a height of a material filling the trench above the semiconductor substrate.

REMARKS

Favorable consideration of this application as presently amended is respectfully requested.

Claims 1-6 are presently active, Claim 1 having been amended by way of the present amendment.

In the outstanding Office Action, Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al (U.S. Pat. No. 6,255,166) and Inoue (U.S. Pat. No. 5,559.048). Claims 2, 3, and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al and Inoue in view of Resinger (U.S. Pat. No. 6,137,718). Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al and Inoue and Resinger in view of Agarwal et al (U.S. Pat. No. 6,201,276). Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al and Inoue in view of Fang (U.S. Pat. No. 6,023,085).

According to the features defined in presently amended Clam 1, a height of a charge storage layer (e.g., the silicon oxide film 112 shown in Applicant's Figure 10) above a

semiconductor substrate (e.g. substrate 101) is lower than a height of a material (e.g. silicon oxide layer 132) filling a trench (e.g. one of the element isolation trenches 126) above the semiconductor substrate.

Accordingly, because end portions of the charge storage layer are isolated from other conductive layers by the surrounding trench filling material, it is possible to prevent the electrons in the charge storage layer from diffusing from the end portions of the charge storage layer to other conductive layers. As a result, the charge retention characteristics of the charge storage layer are improved.

Inoue discloses a double layered floating gate EPROM having a first floating gate 103, a second floating gate 106, and a control gate 110. Electrons are charged into the first floating gate 103. However, the second floating gate 106 is formed on the first floating gate 103 directly, thus the electrons charged in the first floating gate 103 diffuse from the first floating gate 103 to the second floating gate 106. In Inoue, the height of the first and second floating gates 103 and 106 over the substrate 101 ***is not lower than*** the height of the trench groove isolation film 108 filling the trench groove 107 over the substrate 101.

That is, the end portions of the first and second floating gates 103 and 106 as shown in Figure 9G of Inoue are not isolated by the trench groove isolation film 108. As a result, Applicant submits that it is not assured in Inoue that electrons existing in the first and second floating gates 103 and 106 will not diffuse to other conductive layers, such as for example diffuse to the nearby polysilicon film layer 110. Hence, the charge retention characteristics of Inoue will be low compared to the charge storage layer of the non-volatile semiconductor memory defined in Claim 1.

Ogura et al do not disclose trench isolation. Accordingly, Ogura et al do not disclose or suggest the above noted feature regarding the height of the charge storage layer relative to the height of the trench filling material.

M.P.E.P. §2143.03 requires to establish *prima facie* obviousness that all the claim limitations must be taught or suggested by the applied prior art. With no features disclosed or suggested in the applied prior art of Ogura et al and Inoue for the claimed charge storage layer defined in Claim 1, a case of *prima facie* obviousness has not been established.

Thus, it is respectfully submitted that Claim 1 and Claims 2-6 which depend from Claim 1 are not obvious and patentably define over the applied prior art.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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Marked-Up Copy
Serial No: 09/955,076
Amendment Filed on: May 8, 2003

IN THE CLAIMS

Please amend Claim 1 as shown below:

1. (Twice Amended) A nonvolatile semiconductor memory comprising:

a semiconductor substrate;

a first transistor formed on a surface of said semiconductor substrate and including a first gate insulating film and a first gate electrode;

a second transistor formed on the surface of said semiconductor substrate and including a second gate insulating film and a second gate electrode; and

a charge storage layer included in said first gate insulating film and absent from said second gate insulating film,

wherein said first and second transistors are isolated by a trench, [and] said charge storage layer in said first transistor is restricted from an element isolation region and exists only below said first gate electrode in an element region, and a height of said charge storage layer above the semiconductor substrate is lower than a height of a material filling the trench above the semiconductor substrate.